**International Journal of Electrical and Electronics Research** ISSN 2348-6988 (online)
Vol. 6, Issue 1, pp: (11-18), Month: January - March 2018, Available at: www.researchpublish.com

# 2A Current Regulation Loop With a Metal Sense Resistor

[1]Sri Navaneeth Easwaran, [1]Sunil Kashyap Venugopal, [1]Deepak Sreedharan, [2]Samir Camdzic, [3]Robert Weigel

[1]Texas Instruments, Dallas, Texas, USA
[2] Texas Instruments, Freising, Germany
[3] Lehrstuhl für Technische Elektronik, University of Erlangen-Nurnberg, Erlangen, Germany

***Abstract:*** **The current regulation loop presented here controls squib drivers that are used to inflate multiple airbags in cars. Conventional approach uses an integrated poly resistor or sense transistor based current sensing, depending on the current range. In this paper, a current regulating High Side Driver (HSD) using an Aluminium metal sense resistor is proposed. This approach of using a metal resistor is new and is fabricated in a 40V, BiCMOS process. HSD is activated for 0.5ms and the current is regulated to 2A from a 33V supply. Regulation is within +/-10% variation despite 400ºC rise on the junction temperature of the power transistor. This design incorporates a new technique to provide an on-chip free-wheeling path due to inductive flyback when the HSD turns OFF, avoiding external Schottky diodes. This approach could be widely used for all current limitation circuits.**

***Keywords:*** **Current sense, squib driver, LDMOS (Laterally Diffused MOS), metal resistor, self-heating, flyback.**

## I. INTRODUCTION

In airbag squib drivers, regulated current of ~ 2A is provided for defined dwell time (~0.5ms) [1] to deploy airbags. Regulated current that is delivered to the squib is accomplished by a High Side Driver (HSD) which drives a power transistor (HS_FET). The Low Side Driver (LSD) drives the second power transistor (LS_FET) that operates as a resistor ($r_{ds\_on}$). This typical airbag deployment loop is shown in Fig. 1. To regulate the current in the range of 100mA to 400mA, sense resistor (integrated poly resistor) [2] is used. Since poly resistor is too large to be integrated for currents in the order of 2A, sense transistor [3] based approach is used. This approach lacks precision due to mismatch effects. For currents above 500mA, poly resistor approach is area-inefficient, while the sense transistor approach is not precise. To meet the precision and area efficiency, Aluminium-based metal sense resistor is proposed here. The targeted current is 2A+/-10% for 0.5ms dwell time. These powerFETs (Field Effect Transistors) are 40V rated LDMOS (Laterally Diffused Metal Oxide Semiconductor) transistors. Squibs are electrical R-L-C networks with resistance ranging from 1Ω to 8Ω. The inductance ranges from 1µH to 100µH and the capacitance from 22nF to 220nF. Deployment supply VZx is 33V and gate driver supply Vdd is at 35V.

## II. CURRENT SENSING AND LIMITATION

### *A. Existing solution-1, Resistor at the source of HS_FET:*

Conventional current regulator circuits use an Operational Transconductance Amplifier (OTA) to regulate the current sensed by the integrated poly resistor ($R_{shunt}$) at the source of the HS_FET as shown in Fig. 2a. In this approach, integrating wide poly resistors for 2A current is not area efficient. Current sensing at the source of the HS_FET is affected by ground shifts, inductive flyback where VZx voltage below ground can trigger undesired parasitic on-chip bipolar transistors. This will affect the accuracy or the stability of the current regulation loop. To overcome this, sense transistor approach is needed.

***B. Existing solution-2, Sense transistor approach:***

The second approach shown in Fig. 2b with a sense transistor MNx whose gate and source are connected to the HS_FET is a good approach to avoid the parasitic currents, but suffers from threshold mismatch [4] effects between power and sense transistor (M:1 ratio) impacting the accuracy of regulated current. Precision of +/-10% is not achievable if dedicated on chip trim is not available to overcome the mismatch issue.

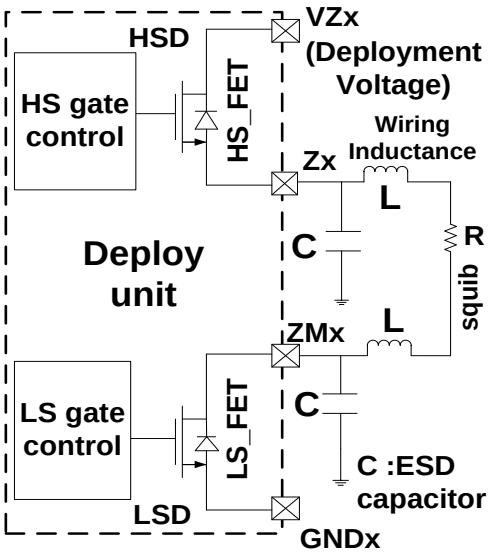



**Fig. 1 Deploy Stages with the squib**

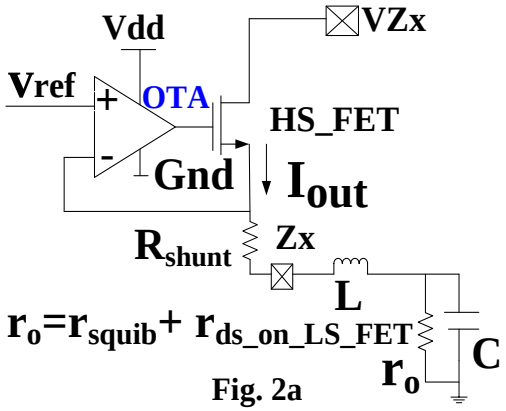



**Fig. 2a. HS_FET Current Regulation- Regulation with resistor on the source of the HS_FET**

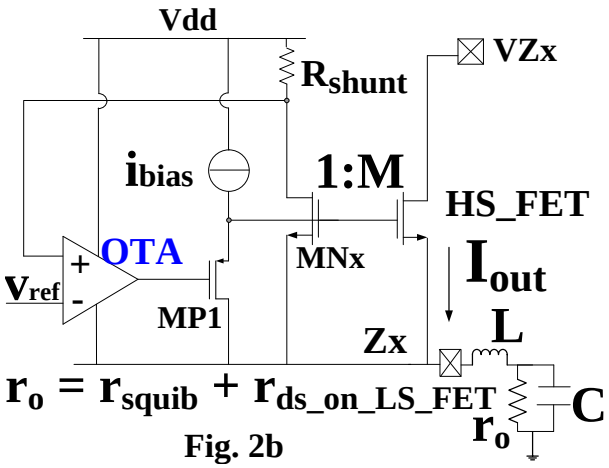



**Fig. 2b. HS_FET Current Regulation- Regulation with sense transistor topology**

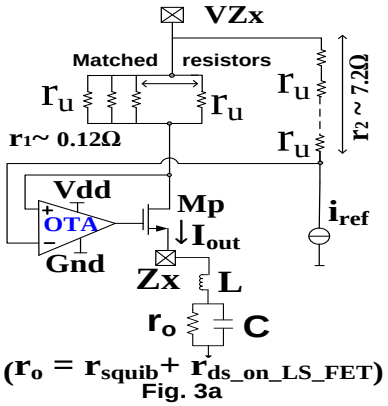



**Fig. 3a. Proposed Current Sensing Scheme**

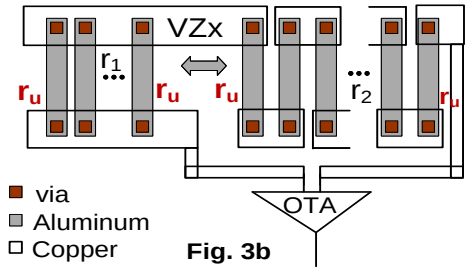



**Fig. 3b. Metal resistor layout**

### *C. Proposed Solution:*

The proposed current regulation shown in Fig. 3a consists of a metal sense resistor on the drain of the HS_FET [5]. Analysis showed that metal resistor is 2x smaller than an integrated poly resistor. The voltage drop across metal resistor $r_1$ is compared with a reference voltage across $r_2$, generated from reference current $i_{ref}$ order to regulate the current. The reference current derived from Bandgap is the only trim needed in order to make this current independent of process variations. Since the sense resistor is on the drain, this approach eliminates potential parasitic currents affecting the regulation loop.

$$I_{out} = i_{ref} \cdot \frac{r_2(1+\Delta t)}{r_1(1+\Delta t)} + \frac{\Delta V_{offset}}{r_1(1+\Delta t)} \sim 33.33mA * 60 \sim 2A$$

The ratio $r_2/r_1$ (~60) determines the current $I_{out}$. The error due to the offset of the OTA is negligible. Good matching of the metal resistors is achieved with the layout scheme [5] shown in Fig. 3b. $r_1$ and $r_2$ are chosen wide enough to handle 33.3mA and 2A respectively. Copper is used as interconnect due to its low resistivity. Thermal simulations ensure the device (WxL) chosen for operation is within the thermal SOA [6] limits. In Fig. 4 thermal simulations indicate that for 2A and 0.5ms deployment pulse at 35V, junction temperature rise in the HS_FET and OTA is around 430ºC and 235ºC respectively. The regulation loop is designed to be stable at such high temperatures.

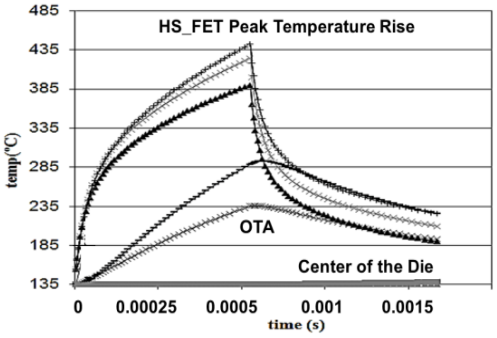


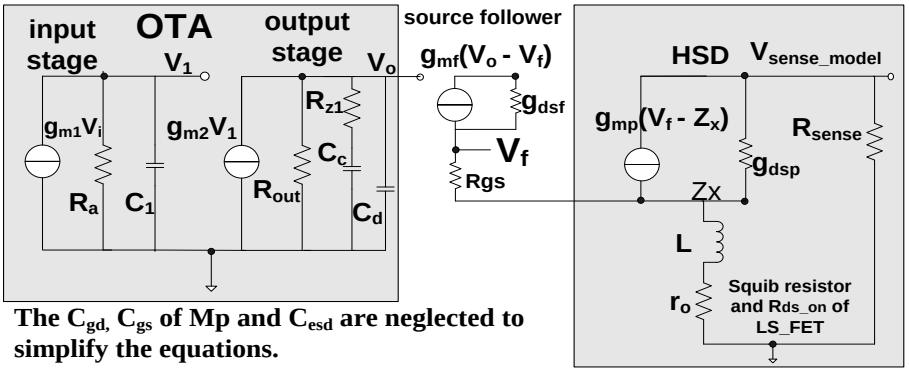

**Fig. 4 Simulated Junction Temperatures on the die**

*Small Signal Analysis:* The stability analysis of this current regulation loop can be performed through the small signal model [7] is shown in Fig. 5. The OTA is represented as a two stage amplifier with first stage transconductance $g_{m1}$ and output impedance $R_a$. Second stage transconductance is $g_{m2}$, output impedance $R_{out}$. HS_FET transconductance is $g_{mp}$. OTA sets the dominant pole ($R_aC_1 << R_{out}C_c$), the second pole is set by $r_o$ and L. $g_{mf}$ and $R_{gs}$ represent the source follower stage. The loop is stabilized by using the capacitor $C_c$ and zeroing resistor $R_{z1}$. Capacitor $C_d$ ensures sufficient damping at high frequencies. The open loop transfer function H(s) ,poles, and zero are derived below. The Bode plot for extreme load variations (1Ω, 100µH – under damped load) and (8Ω,1µH- over damped load) are shown in Fig. 6.

$$When\ r_O > 1\Omega,\ \frac{g_{mp}}{1+g_{mp}r_o} \sim r_o$$

$$H(s) = \frac{g_{m1}R_a g_{m2}R_{out}R_{sense}\left(1+sR_{z1}C_c\right)}{r_o\left[1+sR_{out}C_c+s^2\left(\frac{LR_{out}C_c}{r_o}\right)\right]}$$

$$f_{p1} = \frac{1}{2\pi R_{out}C_c};\quad f_{p2} = \frac{r_o}{2\pi L}\quad ;\quad f_{z1} = \frac{1}{2\pi R_{z1}C_c}\quad ;\quad f_\tau = \frac{g_{m1}R_a g_{m2}R_{sense}}{2\pi r_o C_c};$$




**The $C_{gd}$, $C_{gs}$ of Mp and $C_{esd}$ are neglected to simplify the equations.**

**Fig. 5 Small Signal Model of the HSD with the HS_FET**

$$g_{m1} = 20\mu S, R_a = 20K\Omega, g_{m2} = 30\mu S, R_{out} = 60G\Omega, C_1 = C_2 = 4pF, R_{z1} = 10M\Omega, g_{mf} = 200\mu S,$$

$$R_{dsf} = 3M\Omega, R_{gs} = 100K\Omega, g_{mp} = 3S, R_{dsp} = 5\Omega, R_{sense} = 120m\Omega,\ r_0 = 2\Omega, L = 100\mu H.$$

Open Loop Gain, Poles and Zeros , UGB after Compensation

$$A_{dc} = \frac{\left(20.10^{-6}\right)\left(20.10^{3}\right)\left(30.10^{-6}\right)\left(60.10^{9}\right)(0.12)}{2} = \frac{86400}{2} = 43200$$

$$\Rightarrow A_{dc} = 20\log_{10}(43200) = 92dB$$

$$f_{p1} = \frac{1}{2\pi\left(60.10^{9}\right)\left(4.10^{-12}\right)} = 663\ mHz$$

$$f_{p2} = \frac{2}{2\pi\left(100.10^{-6}\right)} = 3.183\ KHz$$

$$f_{z1} = \frac{1}{2\pi\left(10.10^{6}\right)\left(4.10^{-12}\right)} = 3.98\ KHz$$

$$f_\tau = \frac{\left(20.10^{-6}\right)\left(20.10^{3}\right)\left(30.10^{-6}\right)(0.12)}{2\pi(2)\left(4.10^{-12}\right)} = 28.64\ KHz$$

Phase Margin $\Phi_m = 180° - \arctan\left(\frac{f_\tau}{f_{p1}}\right) - \arctan\left(\frac{f_\tau}{f_{p2}}\right) + \arctan\left(\frac{f_\tau}{f_{z1}}\right)$

$$\Rightarrow \Phi_m = 180° - \arctan\left(\frac{28.64K}{0.633}\right) - \arctan\left(\frac{28.64K}{3.183K}\right) + \arctan\left(\frac{28.64K}{3.98K}\right) = 90°$$

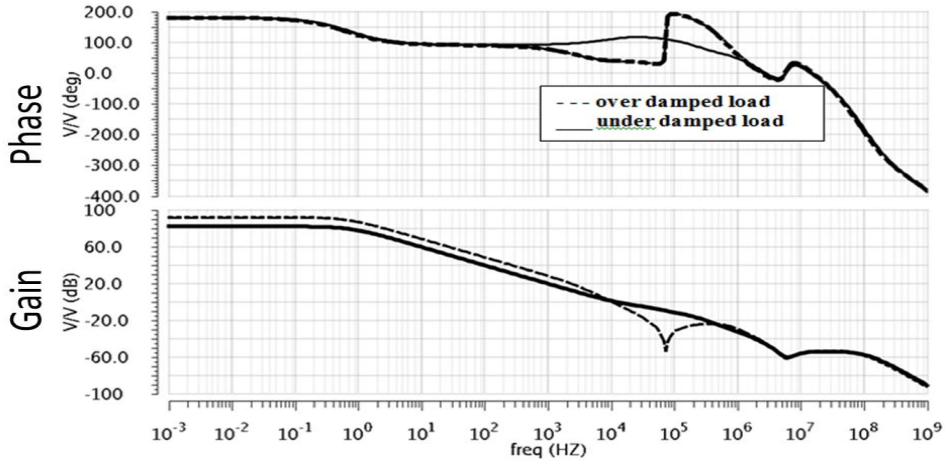



**Fig. 6 Bode Plot for over and under damped loads**

The schematic of current regulation is shown in Fig. 7. The die photo is shown in Fig. 8. The resistor $R_{gs}$ (100KΩ) ensures $V_{gs}$ of HS_FET is lower than its threshold voltage $V_{th}$ to avoid unintended activation of $M_p$ during supply ramps conditions. The diode D2 is a Zener protection for the gate-source junction of $M_p$. The parasitic diode $D_{par}$ clamps the gate of $M_p$ to -0.7V, when VZx flies negative due to the inductive flyback after the HSD is deactivated. Positive $V_{gs}$ on $M_p$, circulates the freewheeling current and avoids external Schottky diodes.

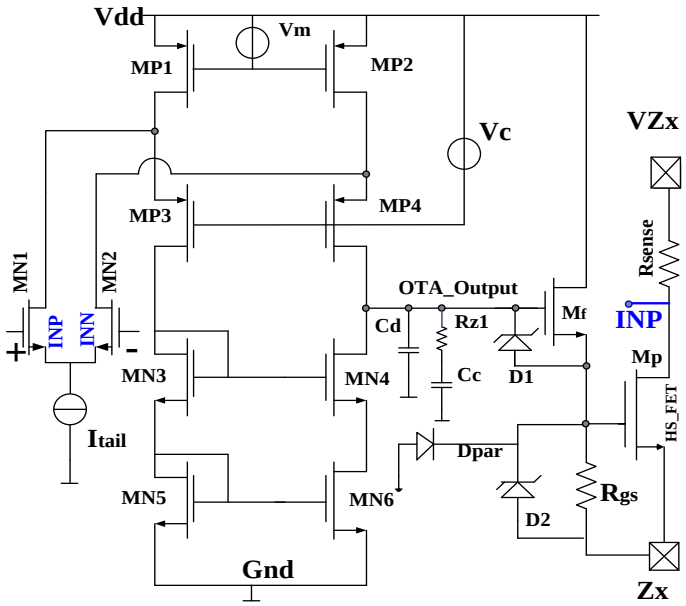



**Fig. 7 HSD with HS_FET and OTA implementation**

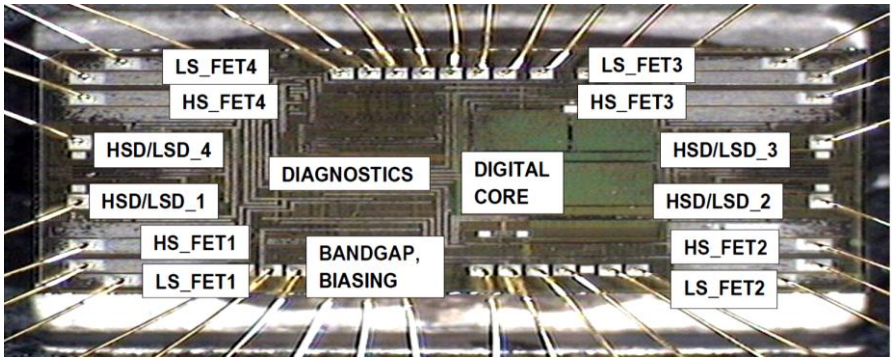



**Fig. 8 Die photo- 4 channel squib driver**

### *D. Measurement Results:*

The metal sense resistor value $r_1$ is chosen to be 120mΩ. However, the width of the metal resistor is critical and should be wide enough to handle the 2A current flow. It should neither be too low nor too high since narrow trace results in Electro Migration whereas the very wide trace is not area and cost efficient. In addition to the regulated currents, the peak currents can be higher when fault conditions like short-to-ground are encountered on the source of the HS_FET. The resistor should also be able to handle these currents. The width of the metal resistor is chosen based on the current density. The current density is defined as the minimum current that can be carried by a 1µm metal trace above which the trace will melt and fuse open. There are three classifications for the current density based on the duration of the current. This is shown in the TABLE I below.

If $J_{DC}$ is used to calculate the metal width, then for 2A level, the metal width has to be 2000µm. This is extremely large area and is not cost effective even for a single driver. To optimize the metal width, the repetition rate of the deployment current pulse should be considered. In Fig. 9, the repetition rate is higher than 500ms with the duty cycle being 700µs for the 2.14A maximum current level or 2ms for the 1.47A maximum current level. $J_{RMS}$ is apt for the Pulse Width Modulation (PWM) based current flow like in switching converters where the switching period is in the order of 1-2µs. The situation considered here indicates the current flow for a short duration through the metal resistor and a long duration where there is no current flow. $J_{RMS}$ is still a non-optimal value for area efficient width of the metal trace. $J_{PEAK}$ is intended for short pulses in "ns" range which is for ESD currents. $J_{PEAK}$ and $J_{RMS}$ based calculations will result in 40µm and 200µm trace widths. The width of 40µm was chosen as this was area efficient.

**TABLE I: CURRENT DENSITY FOR METAL TRACES**

| Types of Current Density | Notation | Thumb Rule mA/µm | Application |
|---|---|---|---|
| PEAK | $J_{PEAK}$ | 50 | ESD (Electro Static Discharge) Currents |
| RMS | $J_{RMS}$ | 10 | PWM (Pulse Width Modulation) Currents |
| DC | $J_{DC}$ | 1 | DC |

### *E. Self-Heating in Metal Resistors*

Since 500µs to 2ms pulse is an intermediate duration between $J_{PEAK}$ and $J_{RMS}$ values, considering $J_{PEAK}$ value to calculate the width of the 120mΩ metal resistor was not sufficient. It turned out that the target on the first design was only 1.78A just barely above the 1.75A when compared to the 2A, $I_{out}$ target. Additional analysis was performed to understand the lowering of the deployment current.

The first step was to check if the $i_{ref}$ current was at its expected level. This current can be checked by measuring the current flowing into the VZx pin when the load is open. This measurement showed that the current was 33.3mA. This indicates that the resistor ratio of 60 was not as expected. It was 50.

Joule's law of heating is one of the driving factors while deciding on the width of the metal trace. This is also known as the Ohmic heating or the resistive heating or self-heating. As power dissipation in the resistor increases, the temperature of the resistor increases causing an increase to the resistance value. This mechanism is called as self-heating. For example, when 2A deployment current flows through the 120mΩ resistor $r_1$, self-heating will cause the resistance $r_1$ to increase. This means that the 120mΩ resistor will increase, causing the output current $I_{out}$ to be lower than 2A. The Heating "H" in Joule is shown by the equation below,

$$H \propto I^2 R t$$

where "I" is the current flowing through the conductor. "R" is the resistance of the conductor and "t" is the time. It is important to ensure that the temperature rise should be well within the melting point of Aluminum ~ 650ºC. Since the heating is proportional to the square of the current flow, the temperature rise has been measured to be instantaneous on the Aluminum metal resistor). The instantaneous heating is approximately within 4µs (the thermal time constant of the Aluminum metal resistor. Hence, the $J_{PEAK}$ value of 50mA is not sufficient to allow 2A flow through the metal. To overcome this limitation an average value between $J_{PEAK}$ and $J_{RMS}$ (~30mA) for current density has been used. This minimizes the impact from self -heating. However, the sense resistor value will decrease and this can be compensated by increasing the reference current. In the current design, the reference current $i_{ref}$ is increased to 40mA to achieve 2A target.

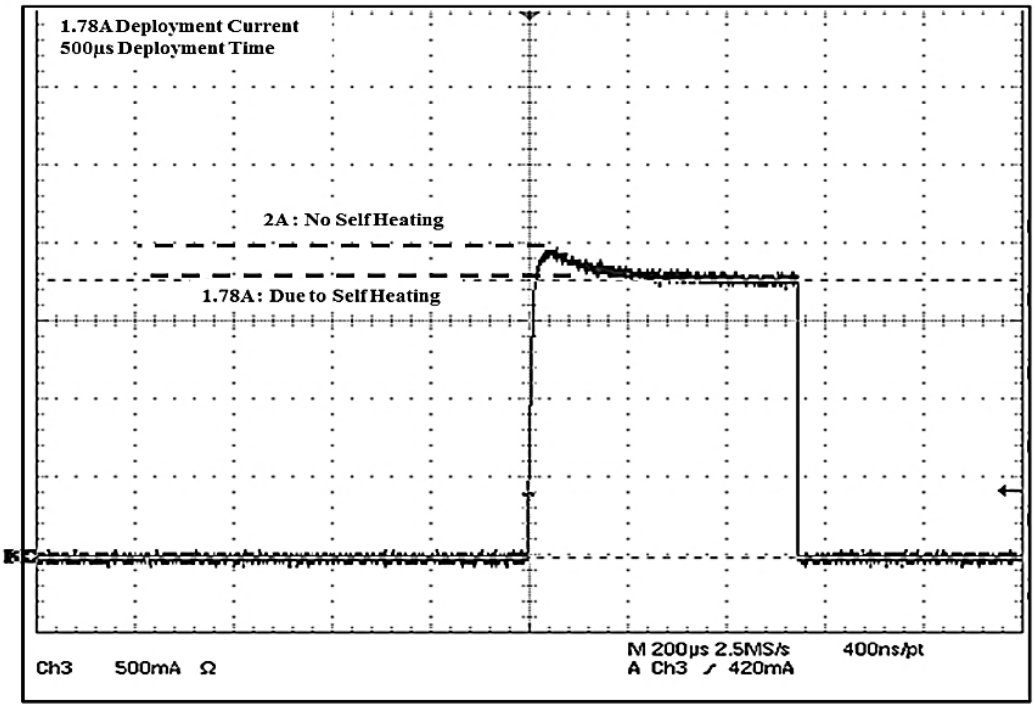



**Fig. 9 Self-heating of metal resistor during deployment**

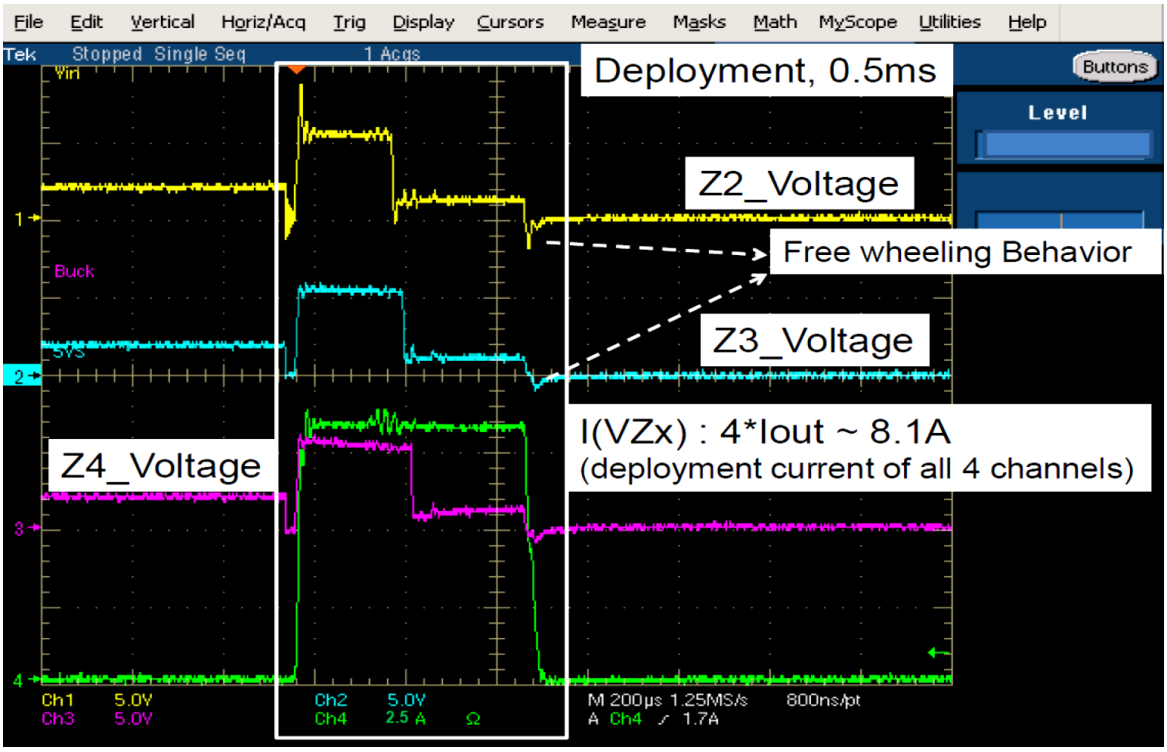



**Fig. 10 Iout , Zx voltages when all 4 loops are deployed simultaneously**

### *F. Measurement Results*

Fig. 10 shows total deployment current of all 4 channels I(VZx) , Z2, Z3 and Z4 voltages for 0.5ms deployment with a 100µH, 1Ω, 22nF load. VZx pins of all 4 channels are connected together and total current I(VZx) is captured here. It is $4*(I_{out} + i_{ref})$ ~ 8.1A. Z1 voltage behaves the same as other Zx pins. After 200µs from the start of deployment, when all ZMx pins were suddenly shorted to ground, $I_{out}$ regulation is very stable for all loops as observed from Fig. 10. Fig. 11 shows $I_{out}$ histogram of channel 1 showing +/-100mA (~ +/-10%) variation. Similar results were obtained for other 3 channels.

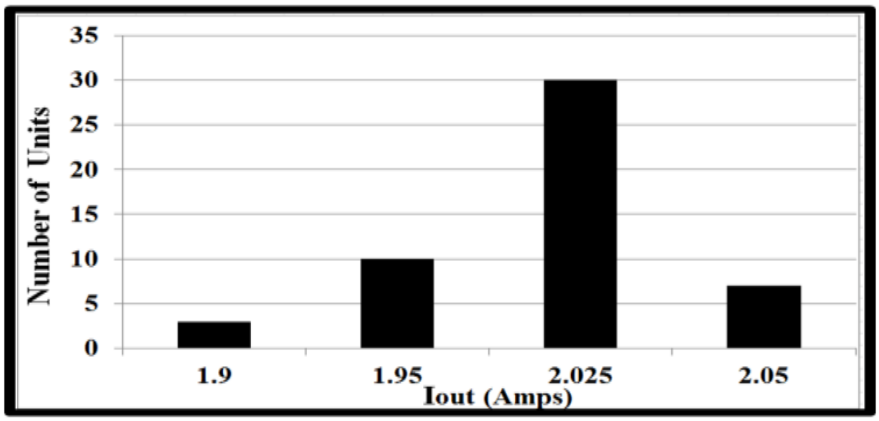



**Fig. 11 Iout ( Deployment current, Channel 1) histogram**

## III. CONCLUSION

The regulation of the deployment current for a High Side Driver (HSD) using metal sense resistor has been successfully implemented in a 4 channel squib driver in a 40V, 0.35µm BiCMOS process. Aluminium metal sense resistor has been used in order to achieve the current regulation within +/-10% precision at a 2x smaller layout area when compared to the poly resistor. The thumb rules to decide on the width of the metal resistor and thermal Safe Operating Area considerations for the powerFET has been presented. Compensating the self -heating effects of the metal resistor by increasing the reference current to achieve 2A target current have been discussed. Even though increasing the reference current does not substantially increase the power dissipation, compensation through the self-heating of the reference resistor might be an alternate solution. If the reference resistor of 7.2Ω is sized slightly narrower such that self-heating dominates, its resistance will increase. This ensures that the ratio between reference and sense resistor does not significantly reduce when compared to the ratio without self-heating. Hence the targeted deployment current without reference current compensation can be achieved. Robust frequency compensation has been implemented. Internal free-wheeling path when the HSD turns OFF is provided by momentarily turning ON the HS_FET. This approach eliminates the need for any external Schottky diodes, especially in multi-channel squib drivers where more than one external Schottky diode would be required.

## REFERENCES

[1] Squib Drivers, TLE6710Q Datasheet, Airbag Combined Power Supply and Firing Circuit, May 4, 2001.

[2] T. Regan, “Current Sense Circuit Collection,” *Linear Technology*, Application Note 105, December 2005.

[3] *Quad Channel Driver for Airbag Deployment*. TPIC71004-Q1, Datasheet, Texas Instruments, SLVSAT2, Feb 2011.

[4] M.J.M. Pelgrom, AAD.C.J. Duinmaijer and A.P.G. Welbers, “Matching Properties of MOS Transistors ,” IEEE Journal of Solid State Circuits, vol. 24,no. 5, pp. 1433-1440.October 1989.

[5] Current Driver Circuit, US Patent, Jan 10, 2012, US 8,093,925B2.

[6] P.L.Hower, “Safe Operating Area - A new frontier in LDMOS Design,” *Proceedings 14th ISPSD and ICs*, Santa FE, New Mexico, June 2002, pp. 1-8, DOI: 10.1109/ISPSD.2002.1016159.

[7] B. Razavi. *Design of Analog CMOS Integrated Circuits*, McGRAW-HILL,NY, USA,2001.